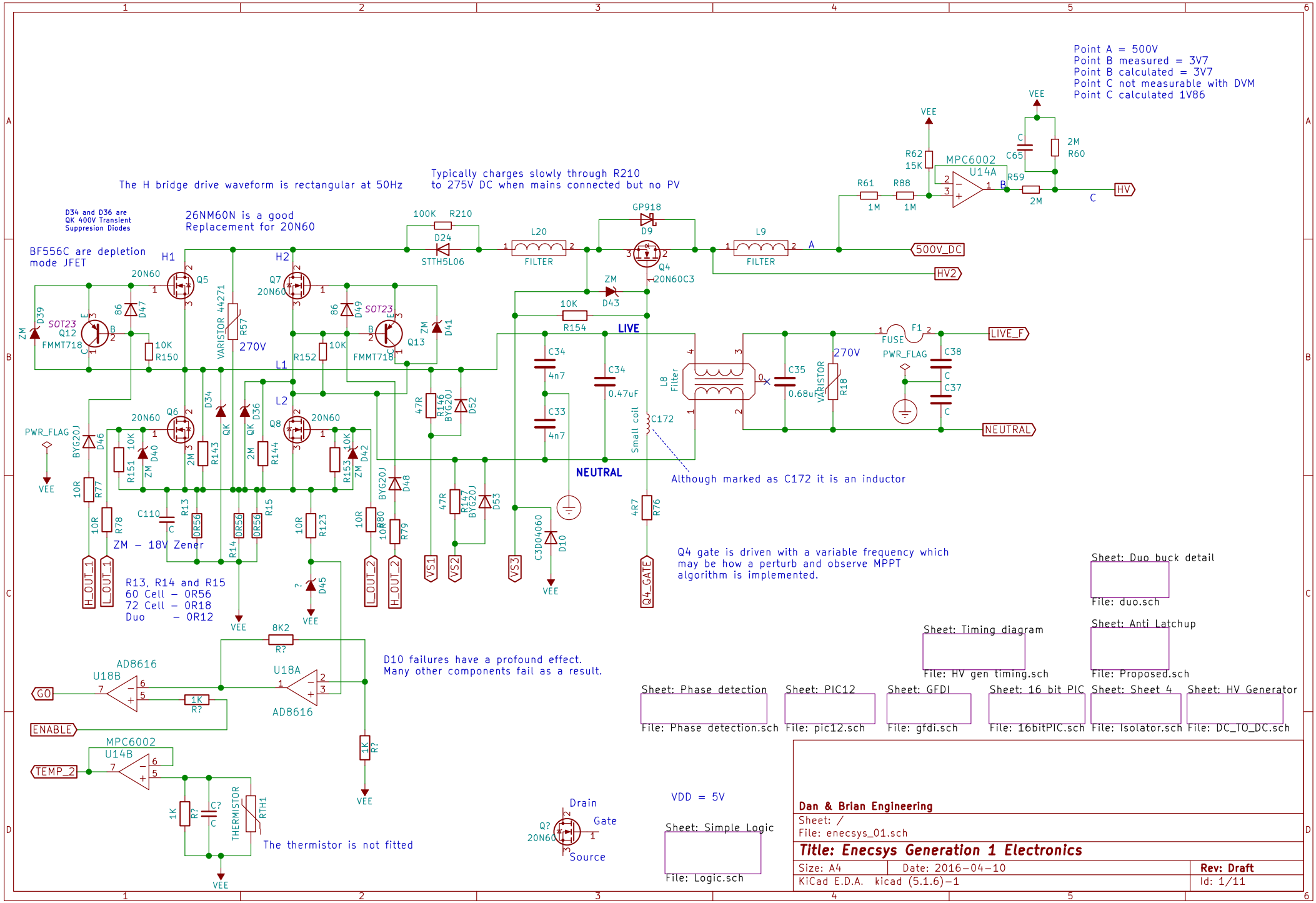
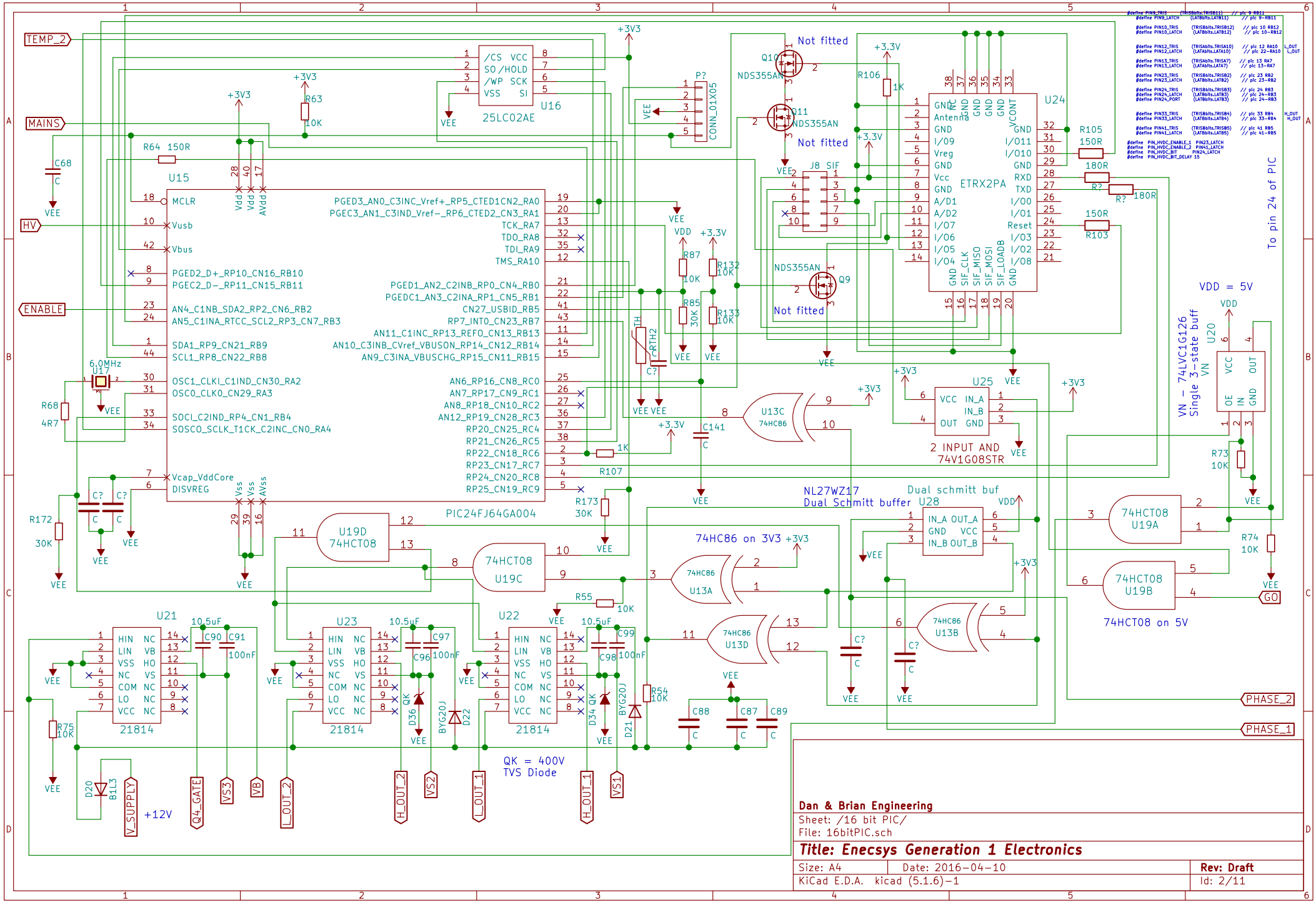
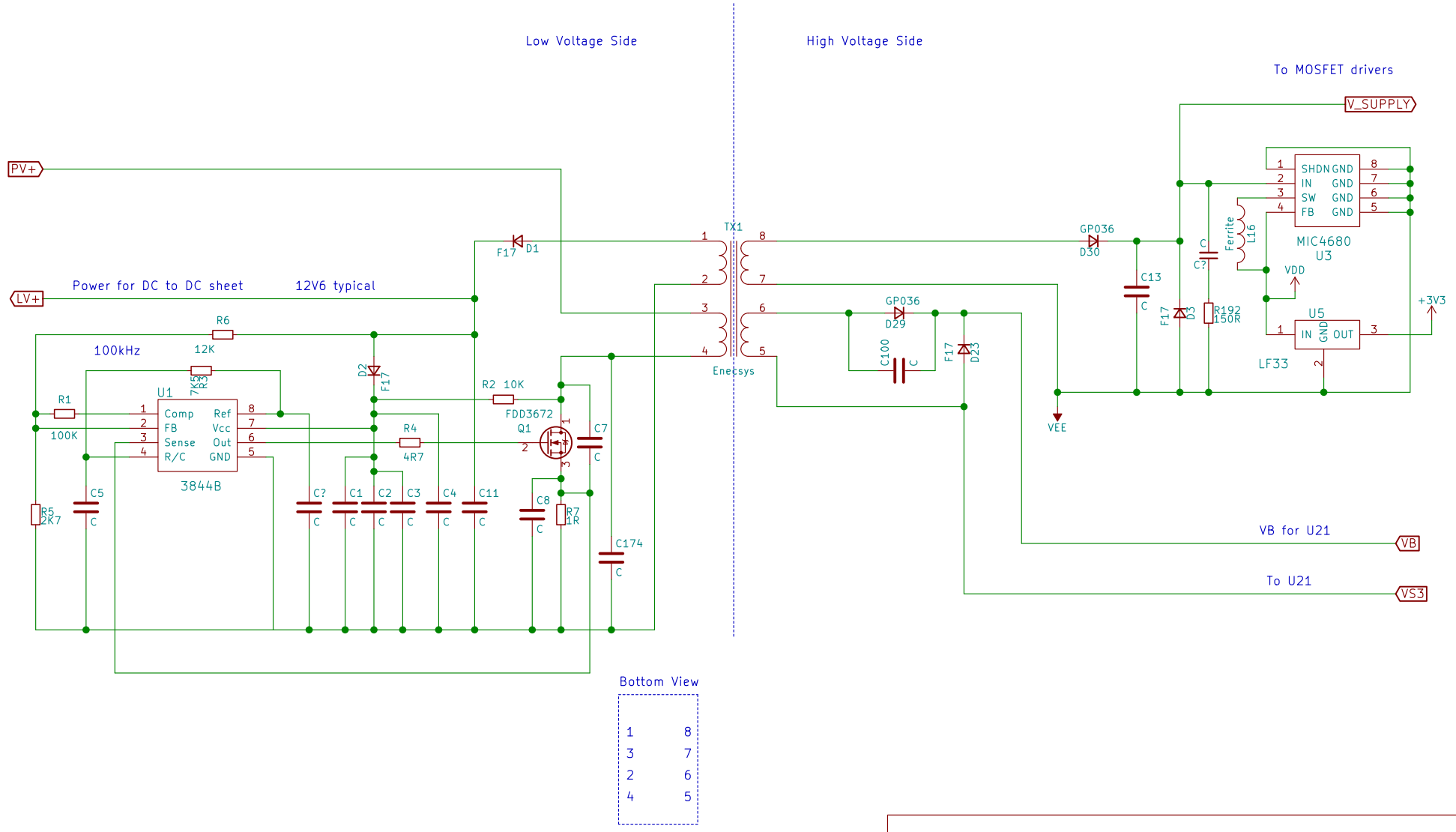

Point A = 500V
Point B measured = 3V7
Point B calculated = 3V7
Point C not measurable with DVM
Point C calculated 1V86
The H bridge drive waveform is rectangular at 50Hz
Typically charges slowly through R210
to 275V DC when mains connected but no PV
D34 and D36 are
QK 400V Transient
Suppresion Diodes
26NM60N is a good
Replacement for 20N60
BF556C are depletion
mode JFET
H1
H2
L1
L2
20N60
Q5
Q7
Q6
Q8
Q12
Q13
FMMT718
SOT23
VARISTOR 44271
R57
270V
R150
R152
R151
R153
R143
R144
R77
R78
R13
R14
R15
R123
R80
R79
R146
R147
BYG20J
D46
D40
D42
D48
D52
D53
D45
D39
D47
D49
D41
D34
D36
ZM
QK
PWR_FLAG
VEE
C110
0R56
10R
47R
ZM – 18V Zener
R13, R14 and R15
60 Cell – 0R56
72 Cell – 0R18
Duo – 0R12
H_OUT_1
L_OUT_1
L_OUT_2
H_OUT_2
VS1
VS2
VS3
Q4_GATE
100K
R210
D24
STTH5L06
L20
FILTER
GP918
D9
Q4
20N60C3
L9
A
500V_DC
HV2
ZM
D43
10K
R154
LIVE
C34
4n7
C33
4n7
C34
0.47uF
NEUTRAL
Small coil
C172
Although marked as C172 it is an inductor
L8
Filter
C35
0.68uF
VARISTOR
R18
270V
FUSE
F1
LIVE_F
PWR_FLAG
C38
C37
NEUTRAL
4R7
R76
C3D04060
D10
Q4 gate is driven with a variable frequency which
may be how a perturb and observe MPPT
algorithm is implemented.
D10 failures have a profound effect.
Many other components fail as a result.
8K2
R?
AD8616
U18B
U18A
GO
ENABLE
1K
R?
MPC6002
U14B
TEMP_2
THERMISTOR
RTH1
The thermistor is not fitted
Drain
Gate
Source
Q?
20N60
VDD = 5V
Sheet: Simple Logic
File: Logic.sch
MPC6002
U14A
R62
15K
R61
1M
R88
1M
R59
2M
R60
2M
C65
C
HV
Sheet: Duo buck detail
File: duo.sch
Sheet: Timing diagram
File: HV gen timing.sch
Sheet: Anti Latchup
File: Proposed.sch
Sheet: Phase detection
File: Phase detection.sch
Sheet: PIC12
File: pic12.sch
Sheet: GFDI
File: gfdi.sch
Sheet: 16 bit PIC
File: 16bitPIC.sch
Sheet: Sheet 4
File: Isolator.sch
Sheet: HV Generator
File: DC_TO_DC.sch
Dan & Brian Engineering
Sheet: /
File: enecsys_01.sch
Title: Enecsys Generation 1 Electronics
Size: A4
Date: 2016-04-10
Rev: Draft
KiCad E.D.A. kicad (5.1.6)-1
Id: 1/11


TEMP_2
MAINS
HV
ENABLE
U15
PIC24FJ64GA004
U16
25LC02AE
U24
ETRX2PA
U25
2 INPUT AND
74V1G08STR
U20
VN – 74LVC1G126
Single 3-state buff
VDD = 5V
To pin 24 of PIC
Not fitted
NDS355AN
Q10
Q11
Q9
J8 SIF
P?
CONN_01X05
U17
6.0MHz
U13C
74HC86
U19D
74HCT08
U19C
74HCT08
U19A
U19B
74HCT08 on 5V
74HC86 on 3V3
U13A
U13D
U13B
NL27WZ17
Dual Schmitt buffer
Dual schmitt buf
U28
U21
U23
U22
21814
QK = 400V
TVS Diode
D20
B1L3
V_SUPPLY
+12V
Q4_GATE
VS3
VB
L_OUT_2
H_OUT_2
VS2
L_OUT_1
H_OUT_1
VS1
PHASE_2
PHASE_1
GO
Dan & Brian Engineering
Sheet: /16 bit PIC/
File: 16bitPIC.sch
Title: Enecsys Generation 1 Electronics
Size: A4
Date: 2016-04-10
Rev: Draft
KiCad E.D.A. kicad (5.1.6)-1
Id: 2/11



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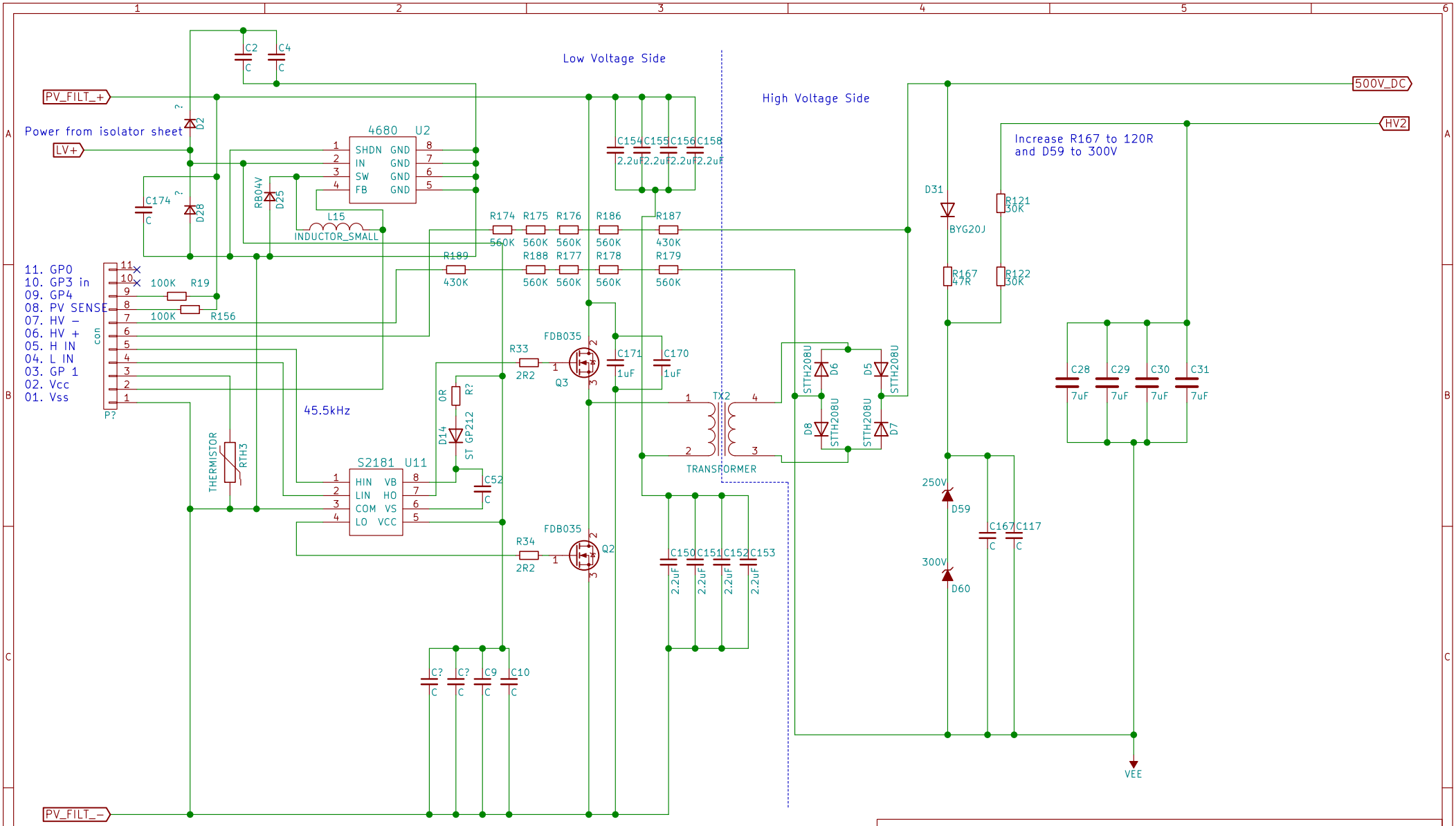
Sheet: /Sheet 4/

File: Isolator.sch

Title: Enecsys Generation 1 Electronics

Size: A4	Date: 2016-04-10	**Rev: Draft**
KiCad E.D.A. kicad (5.1.6)-1		Id: 3/11



Dan & Brian Engineering

Sheet: /HV Generator/

File: DC_TO_DC.sch

Title: Enecsys Generation 1 Electronics

Size: A4	Date: 2016-04-10	**Rev: Draft**
KiCad E.D.A. kicad (5.1.6)-1		Id: 4/11

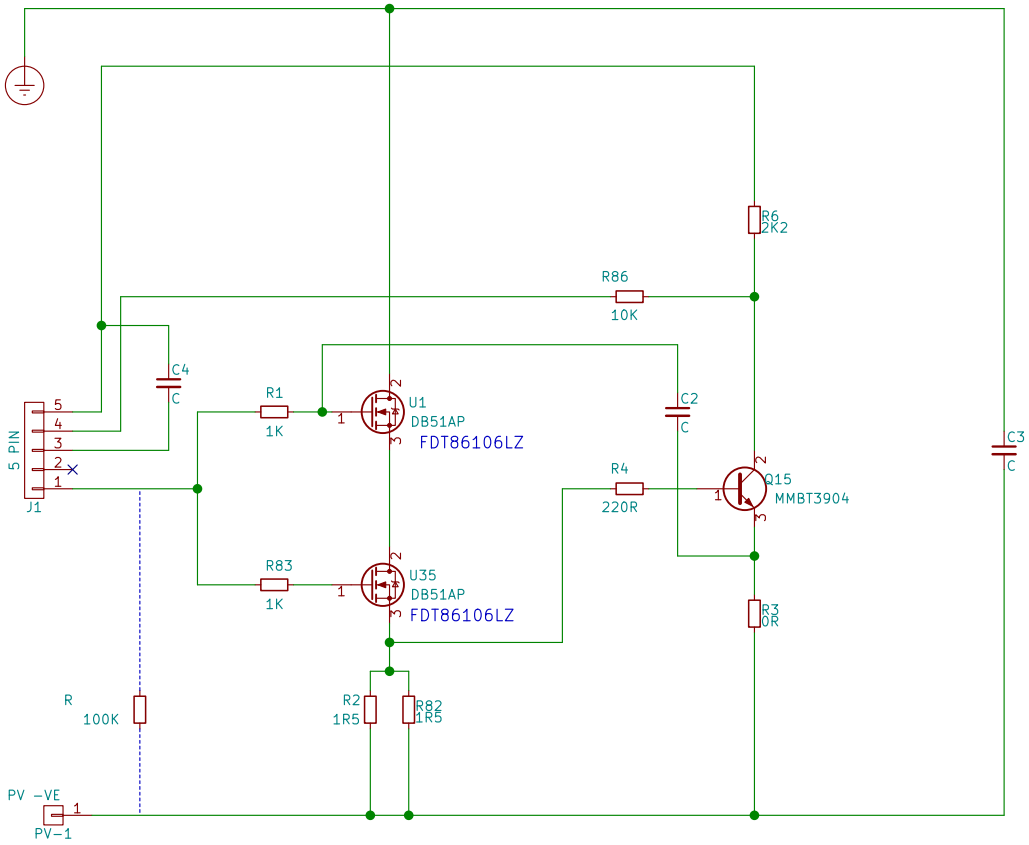
The current plan is for J1 pin 1 to be driven low from PIC12 GP1 to ensure that U1 and U35 do not turn on.

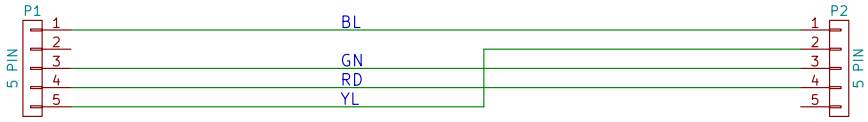
The cable must be fitted

Pickit PCB has 3 LED's:
LED 1 – POWER
LED 2 – GP1
LED 3 – GP0

PIC12 GP0
VCC
VSS
Not Used
PIC12 GP1

J1 pin 1 connects to NTC thermistor RTH3 (10K) on main PCB
RTH3 is a pull down to PV– with min val of 1K at 90 dec C





GFDI END

PIC END

GFDI is not fitted on all units

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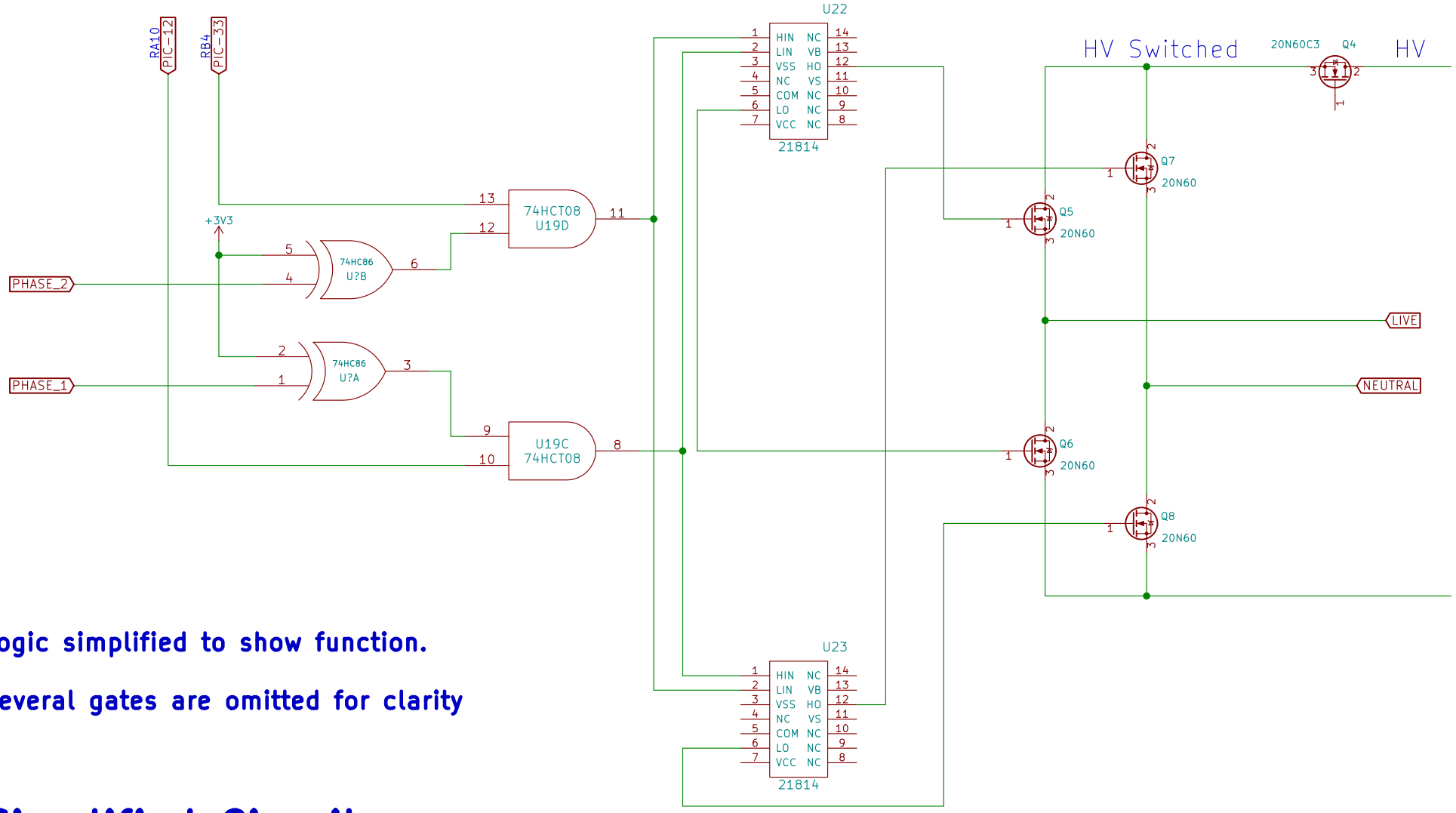
Sheet: /GFDI/
File: gfdi.sch

Title: Enecsys Generation 1 Electronics

Size: A4	Date: 2016–04–10	**Rev: Draft**
KiCad E.D.A. kicad (5.1.6)–1		Id: 5/11



Logic simplified to show function.

Several gates are omitted for clarity

Simplified Circuitry
Does not show full connectivity

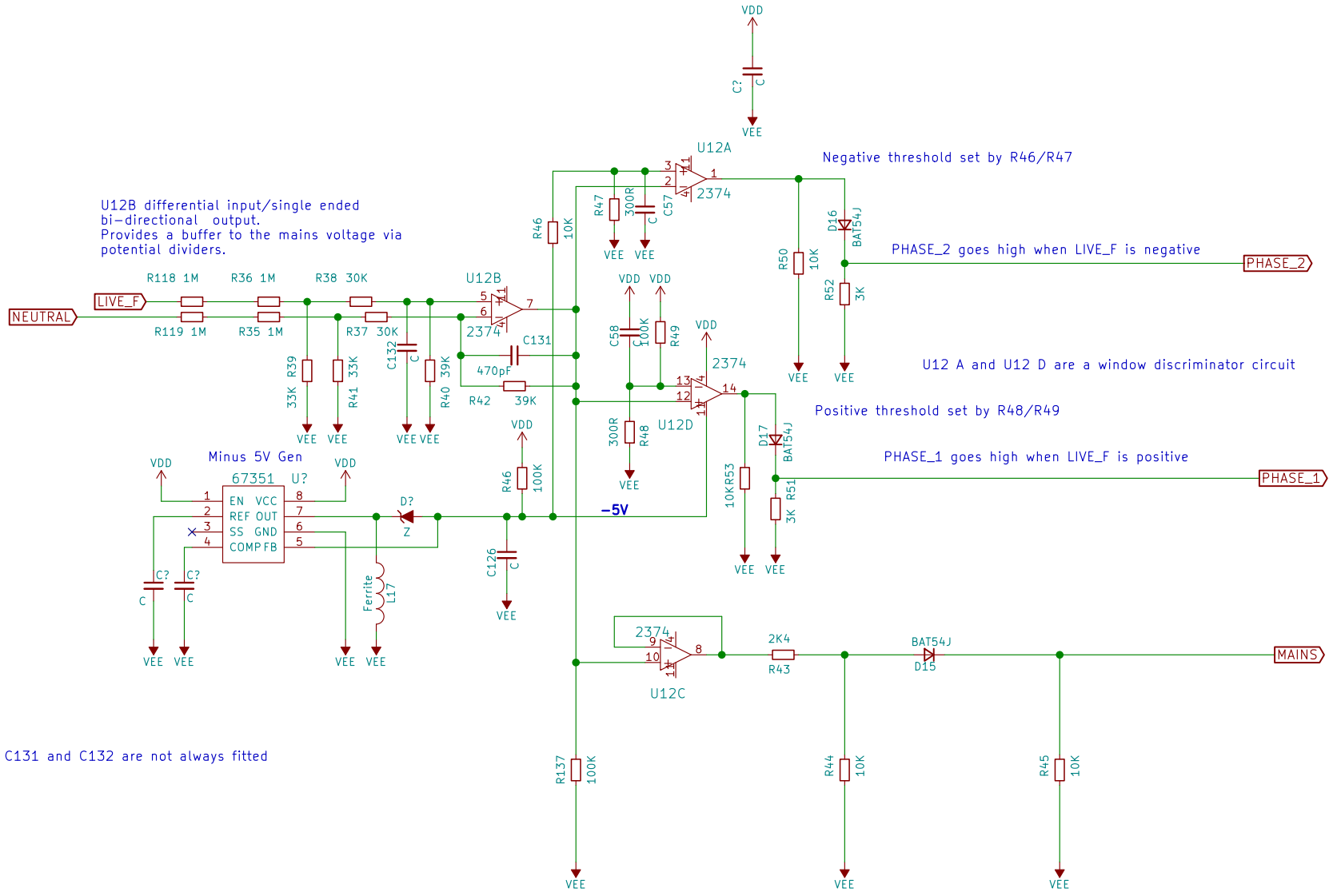
Dan & Brian Engineering

Sheet: /Simple Logic/

File: Logic.sch

Title: Enecsys Generation 1 Electronics

Size: A4	Date: 2016-04-10	**Rev: Draft**
KiCad E.D.A. kicad (5.1.6)-1		Id: 6/11



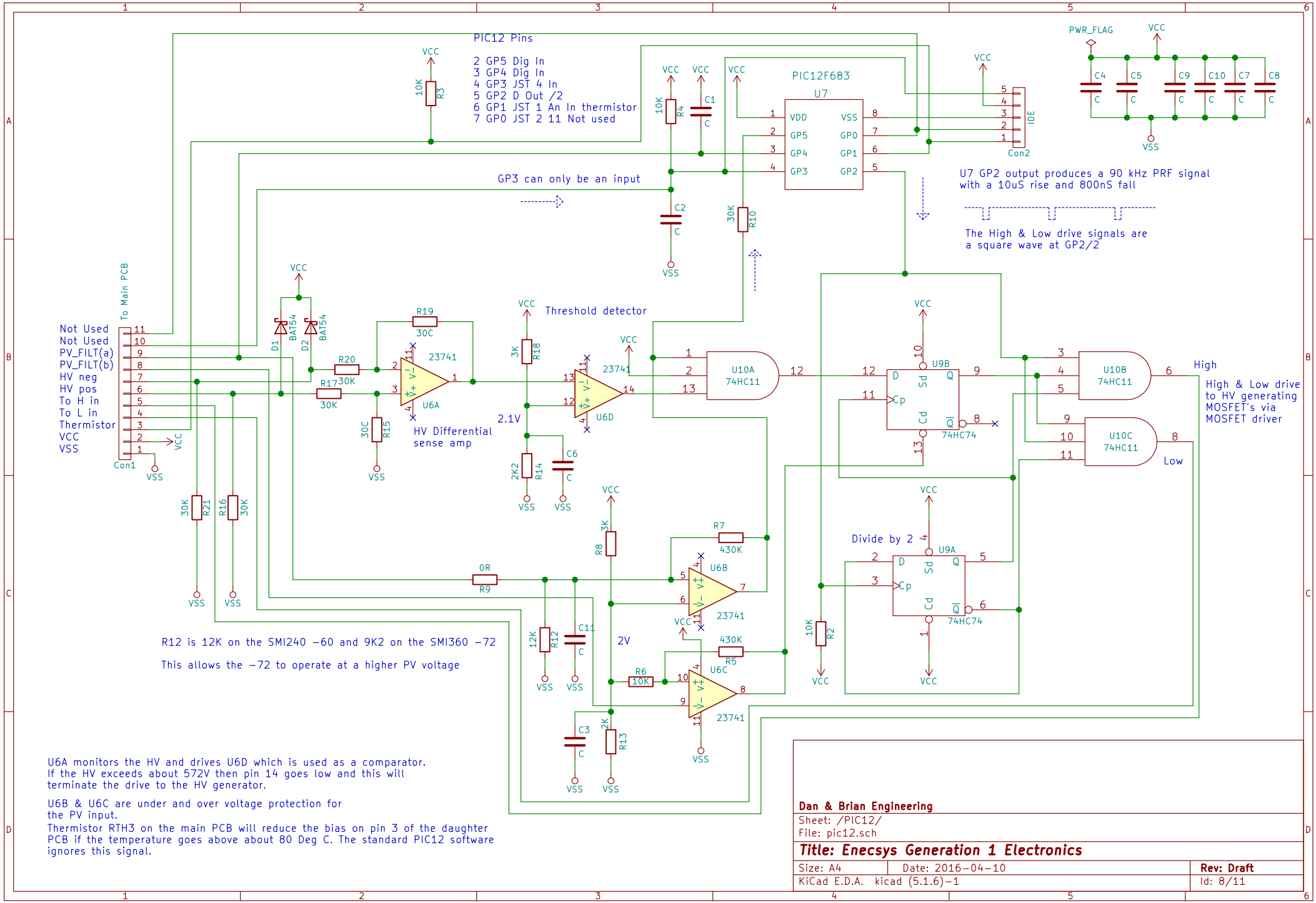
Dan & Brian Engineering

Sheet: /Phase detection/

File: Phase detection.sch

Title: Enecsys Generation 1 Electronics

Size: A4	Date: 2016-04-10	**Rev: Draft**
KiCad E.D.A. kicad (5.1.6)-1		Id: 7/11



R12 is 12K on the SMI240 -60 and 9K2 on the SMI360 -72

This allows the -72 to operate at a higher PV voltage

U6A monitors the HV and drives U6D which is used as a comparator.
If the HV exceeds about 572V then pin 14 goes low and this will
terminate the drive to the HV generator.

U6B & U6C are under and over voltage protection for
the PV input.
Thermistor RTH3 on the main PCB will reduce the bias on pin 3 of the daughter
PCB if the temperature goes above about 80 Deg C. The standard PIC12 software
ignores this signal.

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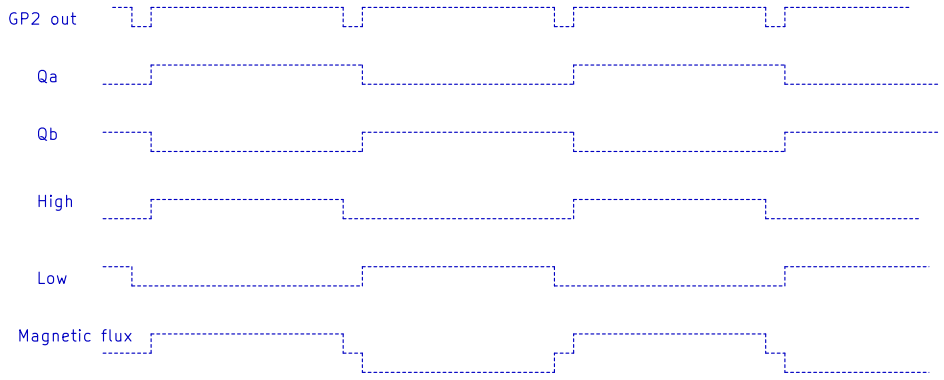
Sheet: /PIC12/
File: pic12.sch

Title: Enecsys Generation 1 Electronics

Size: A4	Date: 2016-04-10	**Rev: Draft**
KiCad E.D.A. kicad (5.1.6)-1		Id: 8/11

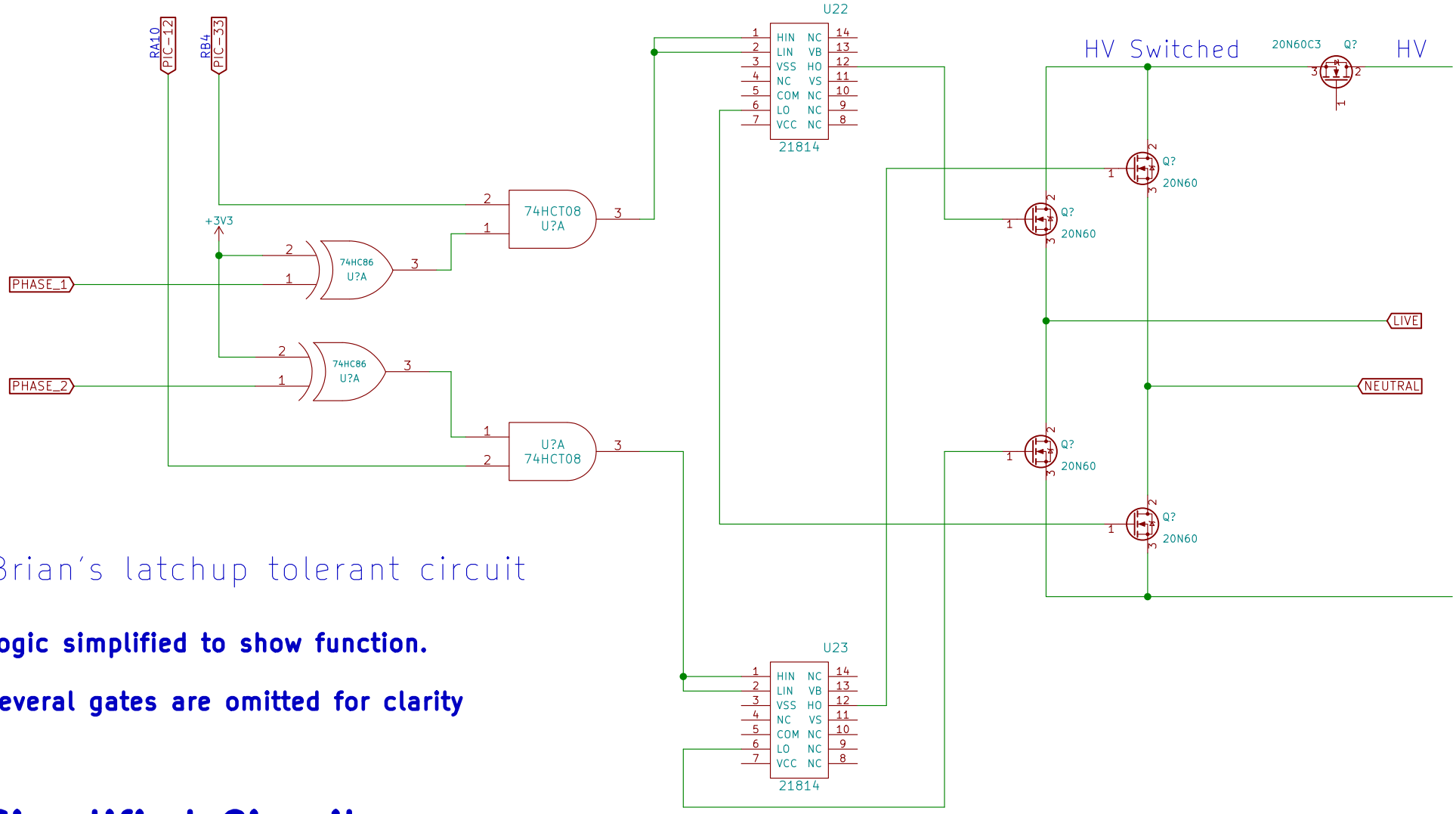
Timing diagram to demonstrate that MOSFET driver U11 cannot experience High side/Low side overlap because an 800nS interval is used to separate the two signals.



Sheet: /Timing diagram/
File: HV gen timing.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.6)-1		Id: 9/11



Brian's latchup tolerant circuit

Logic simplified to show function.

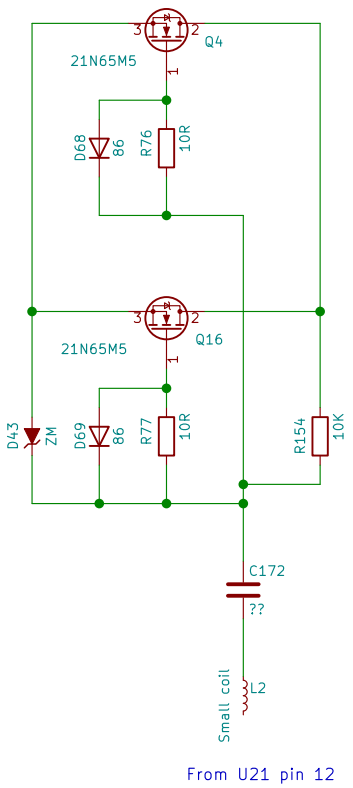
Several gates are omitted for clarity

Simplified Circuitry
Does not show full connectivity

Sheet: /Anti Latchup/
File: Proposed.sch

Title:

Size: A4	Date:	Rev:
KiCad E.D.A. kicad (5.1.6)-1		Id: 10/11



The DUO has two buck MOSFET's.
They are driven from the same U21 pin 12 output
as used on the 60 and 72

Sheet: /Duo buck detail/
File: duo.sch

Title:

Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad (5.1.6)-1		Id: 11/11